## CLAIMS

What is claimed is:

1. A semiconductor package with build-up layers formed on a chip, comprising:

a chip having an active surface and a non-active surface and formed with a plurality of bond pads on the active surface;

a conductive bump formed on each of the bond pads of the chip;

a carrier having a cavity for receiving the chip therein, wherein the non-active surface of the chip is attached to a bottom surface of the cavity, and a depth of the cavity is between a thickness of the chip and a sum of the thickness of the chip and a height of the conductive bump;

a first dielectric layer which is applied over the active surface of the chip and the carrier, and which fills in the cavity and encapsulates the conductive bumps with ends of the conductive bumps being exposed; and

a plurality of first conductive traces formed on the first dielectric layer and electrically connected to the exposed ends of the conductive bumps.

2. The semiconductor package of claim 1, further comprising: a second dielectric layer applied over the first conductive traces and formed with a plurality of vias by which predetermined portions of the first conductive traces are exposed.
3. The semiconductor package of claim 2, further comprising: a plurality of second conductive traces formed on the second dielectric layer and electrically connected to the exposed portions of the first conductive traces.
4. The semiconductor package of claim 3, further comprising: a solder mask layer applied over the second conductive traces and formed with a plurality of openings via which predetermined portions of the second conductive traces are exposed.
5. The semiconductor package of claim 4, further comprising: a solder ball formed on each of the exposed portions of the second conductive traces.

6. The semiconductor package of claim 1, wherein the conductive bump is selected from the group consisting of a solder bump, a gold (Au) bump, and an Au stud bump.
7. The semiconductor package of claim 1, wherein the carrier is made of a non-conductive material.
8. The semiconductor package of claim 1, wherein the carrier is a metallic heat sink.
9. A fabrication method of a semiconductor package with build-up layers formed on a chip, comprising the steps of:

preparing a wafer comprising a plurality of chips, each of the chips having an active surface and a non-active surface and formed with a plurality of bond pads on the active surface;

forming a conductive bump on each of the bond pads of the chips;

singulating the wafer to form a plurality of single chips each having a plurality of the conductive bumps thereon;

providing a carrier having a cavity for receiving at least one of the chips therein, wherein the non-active surface of the chip is attached to a bottom surface of the cavity, and a depth of the cavity is between a thickness of the chip and a sum of the thickness of the chip and a height of the conductive bump;

applying a first dielectric layer over the active surface of the chip and the carrier, wherein the first dielectric layer fills in the cavity and encapsulates the conductive bumps with ends of the conductive bumps being exposed; and

forming a plurality of first conductive traces on the first dielectric layer, and allowing the first conductive traces to be electrically connected to the exposed ends of the conductive bumps.

10. The fabrication method of claim 9, further comprising a step of: applying a second dielectric layer over the first conductive traces and forming a plurality of vias

through the second dielectric layer, so as to allow predetermined portions of the first conductive traces to be exposed by the vias.

11. The fabrication method of claim 10, further comprising a step of: forming a plurality of second conductive traces on the second dielectric layer, and allowing the second conductive traces to be electrically connected to the exposed portions of the first conductive traces.
12. The fabrication method of claim 11, further comprising a step of: applying a solder mask layer over the second conductive traces and forming a plurality of openings through the solder mask layer, so as to allow predetermined portions of the second conductive traces to be exposed via the openings.
13. The fabrication method of claim 12, further comprising a step of: forming a solder ball on each of the exposed portions of the second conductive traces.
14. The fabrication method of claim 9, wherein the first dielectric layer is partly removed to expose the ends of the conductive bumps.
15. The fabrication method of claim 10, wherein the vias of the second dielectric layer are formed by a laser drilling technique.
16. The fabrication method of claim 9, wherein the conductive bump is selected from the group consisting of a solder bump, a gold (Au) bump, and an Au stud bump.
17. The fabrication method of claim 14, wherein the first dielectric layer is partly removed by a mechanical grinding technique to expose the ends of the conductive bumps.
18. The fabrication method of claim 14, wherein the first dielectric layer is partly removed by a chemical etching technique to expose the ends of the conductive bumps.
19. The fabrication method of claim 9, wherein the carrier is made of a non-conductive material.

20. The fabrication method of claim 9, wherein the carrier is a metallic heat sink.